REMARKS

The Office Action dated October 6, 2004, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

By this Amendment, claim 1 has been cancelled and claims 2-7 have been amended. Applicant submits that the amendments made herein are fully supported in the specification and the drawings as originally filed, and therefore no new matter has been added. Accordingly, claims 2-20 are pending in the present application and are respectfully submitted for consideration.

Claims 2-20 Recite Patentable Subject Matter

Claims 1-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Moriwaki et al. (U.S. Patent No. 6,490,715, hereinafter "Moriwaki") in view of Masaki et al. (U.S. Patent No. 5,680,064, hereinafter "Masaki"). Claim 1 has been cancelled, rendering this claim moot with regard to this rejection, and claims 2-7 have been amended. Applicant respectfully traverses the rejection, and submits that each of claims 2-20 recites subject matter that is neither disclosed nor suggested by the cited prior art.

Claim 8 recites a semiconductor device comprising, among other features, a plurality of first standard cells, wherein at least one of the first standard cells is arranged in the first block and at least one of the first standard cells is arranged in the second block, each of the first standard cells having a first power supply terminal; a second standard cell arranged between the first and second blocks, wherein the second standard cell has a second power supply terminal misaligned with the first power supply

terminal; and at least one level converter cell aligned with the first and second standard cells and having a third power supply terminal aligned with the first power supply terminal and a fourth power supply terminal aligned with the second power supply terminal.

Claim 16 recites a designing apparatus for generating layout data of a semiconductor device, wherein the semiconductor device comprises, among other features, wherein each of the first standard cells have a first power supply terminal formed in the first region, the second standard cell has a second power supply terminal formed in the second region, and the level converter cell has a third power supply terminal formed in the first region and a fourth power supply terminal formed in the second region.

Claim 19 recites a computer readable storage medium storing a program for generating layout data of a semiconductor device having, among other features, wherein each of the first standard cells have a first power supply terminal formed in the first region, the second standard cell has a second power supply terminal formed in the second region, and the at least one level converter cell has a third power supply terminal formed in the first region and a fourth power supply terminal formed in the second region.

Claim 20 recites a semiconductor device comprising, among other features, a plurality of first standard cells arranged in each of the first and second blocks, wherein each of the plurality of first standard cells has a predetermined shape and includes an end and a first power supply terminal formed at a location separated from the end by a predetermined first distance, the first power supply terminal being connected to the first

power supply line; a second standard cell having substantially the same shape as the first standard cells and including an end and a second power supply terminal formed at a location separated from the end by a predetermined second distance that differs from the first distance, the second power supply terminal being connected to the second power supply line; and a level converter cell aligned with the first and second standard cells, wherein the level converter cell has substantially the same shape as the first and second standard cells and includes an end, a third power supply terminal formed at a location separated from the end by the first distance and connected to the first power supply line, and a fourth power supply terminal formed at a location separated from the end by the second distance and connected to the second power supply line.

It is respectfully submitted that the prior art fails to disclose or suggest at least the above-mentioned features of the Applicants' invention.

The Office Action characterized Moriwaki as allegedly disclosing "a semiconductor device comprising: (a) a plurality of blocks including a first block and second block (Fig. 2); (b) the use of standard cells (col. 2, lines 31-53); (c) a level converter cell (Figs. 5A and 5B). " The Office Action further alleges that, "Masaki recites all the other claimed elements."

Applicants submit that Moriwaki and Masaki, taken alone or in combination, fails to disclose or suggest each and every element recited in claims 8, 16, 19 and 20 of the present application. In particular, it is submitted that the cell library database and design aiding system of Moriwaki and the level converter of Masaki, do not disclose at least the structural features and layout of the power supply terminal as claimed.

For example, each of claims 8, 16, 19 and 20 includes a first standard cell having a first power supply terminal, a second standard cell having a second power supply terminal, and a level converter cell having third and fourth power supply terminals. The first power supply terminal of the first standard cell is aligned with the third power supply terminal of the level converter cell. The second power supply terminal of the second standard cell, which terminal is misaligned with the first power supply terminal, is aligned with the fourth power supply terminal of the level converter cell. Accordingly, the four power supply terminals of the present invention, for example, are laid out in two straight lines. This layout enables supplying a level converter cell with a power from a power supply line that is arranged in a layer in which a power supply terminal is arranged, even if the semiconductor device does not have a lattice-form power supply line network. In contrast, Moriwaki in view of Masaki do not disclose such features.

To establish *prima facie* obviousness, each feature of a rejected claim must be taught or suggested by the applied art of record. See M.P.E.P. §2143.03 and *In re Royka*, 490 F.2d 981 (CCPA 1974). As explained above, Moriwaki and Masaki, alone or in combination, do not teach or suggest each feature recited by pending claims 8, 16, 19 and 20. Accordingly, for the above provided reasons, Applicant respectfully submits that pending claims 8, 16, 19 and 20 are not rendered obvious under 35 U.S.C. § 103 by the teachings of Moriwaki in view of Masaki, and therefore are allowable.

As claims 2-7 and 9-15 depend from claim 8, and claims 17 and 18 depend from claim 16, Applicant submits that each of these claims incorporates the patentable aspects therein, and are therefore allowable for at least the reasons set forth above with

respect to the independent claims, as well as for the additional subject matter recited therein.

Under U.S. patent practice, the PTO has the burden under §103 to establish a *prima facie* case of obviousness. In re Fine, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). Both the case law of the Federal Circuit and the PTO itself have made clear that where a modification must be made to the prior art to reject or invalidate a claim under §103, there must be a showing of proper motivation to do so. The mere fact that a prior art reference could arguably be modified to meet the claim is insufficient to establish obviousness. The PTO can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. Id. In order to establish obviousness, there must be a suggestion or motivation in the reference to do so. See also In re Gordon, 221 USPQ 1125, 1127 (Fed. Cir. 1984) (prior art could not be turned upside down without motivation to do so); In re Rouffet, 149 F.3d 1350 (Fed. Cir. 1998); In re Dembiczak, 175 F.3d 994 (Fed. Cir. 1999); In re Lee, 277 F.3d 1338 (Fed. Cir. 2002). The Office Action restates the advantages of the present invention to justify the combination of references. There is, however, nothing in the applied references to evidence the desirability of these advantages in the disclosed structure.

Applicant respectfully requests withdrawal of the rejection.

Conclusion

In view of the above, Applicant respectfully submits that each of claims 2-20 recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicant also

submits that this subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore, respectfully requests that claims 2-20 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, **referencing docket number 108075-00062.**

Respectfully submitted,

Sam Huang
Attorney for Applicant
Registration No. 48,430

Customer No. 004372
ARENT FOX, PLLC
1050 Connecticut Avenue, N.W., Suite 400
Washington, D.C. 20036-5339
Tel: (202) 857-6000
Fax: (202) 638-4810

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Enclosure: Petition for Extension of Time

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